



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Aveek Sarkar et al.

Title: METHOD AND SOFTWARE FOR IMPROVED CIRCUIT PATH TIMING  
PREDICTIONS, AND CIRCUIT DESIGN PRODUCED THEREWITH

Application No.: 10/651,113

Filed:

August 28, 2003

Examiner: (Unassigned)

Group Art Unit:

2858

Atty. Docket No.: 004-8907

Confirmation No.:

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September 19, 2005

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**37 C.F.R. § 1.97(b)**

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- ☐ Form(s) PTO/SB/08A (N/A page(s), with copy of no reference(s)).
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- ☐ Other: N/A

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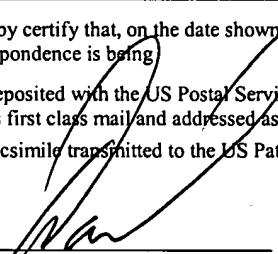
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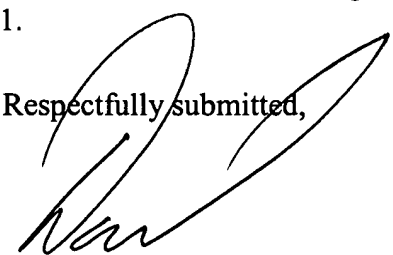
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- ☐ This Information Disclosure Statement is filed within three months of the filing date of a national application other than a continued prosecution application under § 1.53(d) or within three months of entry of the national stage as set forth in § 1.491 in an international application. Therefore, no fee is required.
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If however, this Information Disclosure Statement is filed after the period specified in § 1.97(b), the undersigned hereby authorizes the Commissioner to charge the fee set forth in § 1.17(p) to Deposit Account No. 50-0631.

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Respectfully submitted,

  
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		Application No.: 10/651,113	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		First Named Inventor: Aveek Sarkar et al.	
		Filing Date: August 28, 2003	
		Group Art Unit: 2858	
		Examiner Name: (Unassigned)	
Sheet 1 of 1		Date Submitted: September 19, 2005	
<b>NON PATENT LITERATURE DOCUMENTS</b>			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of author (in CAPITAL LETTERS), title of article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		"Synopsys and Texas Instruments", product description, 6 pages, Synopsys, Inc., copyright 1999.	
		Yalcin, et al. "An Advanced Timing Characterization Method Using Mode Dependency", Proceedings of the 38th Conference on Design Automation (DAC'01), pp. 657-660, June 18-22, 2001.	
		Agah, Hamid, "Physical Synthesis", Application Note: FPGAs, from XILINX®, XAPP140, (v1.0), 3 pages, Xilinx, Inc., February 26, 2001.	
		"PathMill: Transistor-Level Static Timing Analysis", 3 pages, Synopsys Products & Solutions, Synopsys, Inc., downloaded from <a href="http://www.synopsys.com/products">http://www.synopsys.com/products</a> , on or about May 2003.	
		Bray, Jeffrey, Sr., "Verifying timing of external IP key to SoC success", EE Times, May 28, 2002, 3 pages, downloaded from <a href="http://www.eetimes.com">http://www.eetimes.com</a> , May 14, 2003.	
		"Transistor and gate level full chip timing analysis and automatic block characterization", product description from Dyna, 3 pages, downloaded from <a href="http://www.circuitsemantics.com">www.circuitsemantics.com</a> , May 14, 2003.	
		"PrimeTime Synopsys Static Timing Solution", 13 pages, 07/29/99, Revision 1.9, Synopsys Products & Solutions, Synopsys, Inc., downloaded from <a href="http://www.synopsys.com/products">http://www.synopsys.com/products</a> on June 5, 2003.	
Examiner Signature		Date Considered	

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